REMARKS:

Claims 1 and 54 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. 6,417,504 (Kozlowski). In response, Applicants respectfully contend that claims 1 and 54 are patentable over Kozlowski for the following reasons.

Claim 1 recites a sensing apparatus including at least one sensor cell (configured to produce a sensor current indicative of a sensed value) and a readout circuit. The readout circuit has an input node coupled to receive the sensor current, an output node, and output voltage generation circuitry (between the input node and output node) configured to generate an output voltage in response to the sensor current while clamping the input node at a potential that is at least substantially fixed.

Claim 54 recites a method for reading out a sensor cell, comprising the steps of asserting a sensor current (indicative of a sensed value) from the sensor cell to an input node of a readout circuit; and operating the readout circuit in response to the sensor current to generate an output voltage (indicative of the sensed value) while clamping the input node at a potential that is at least substantially fixed.

Kozlowski discloses circuits, each having a portion (including photodiode PD1, PD2, or PD3) that arguably corresponds to the recited sensor cell. One such circuit is shown in Kozlowski's Fig. 1 and described as the "generalized circuit in accordance with [Kozlowski's] invention." The others (e.g., those of Figs. 2 and 3) are said to be specific embodiments, apparently of the generic circuit of Kozlowski's Fig. 1.

The circuit of Kozlowski's Fig. 1 includes buffer amplifier A1 (and circuitry coupled to amplifier A1's output) for reading out photodiode PD1. There is no teaching or suggestion in Kozlowski that photodiode PD1 asserts a sensor current to amplifier A1. On the contrary, Kozlowski teaches that amplifier A1 amplifies the voltage at its input (which is the voltage across PD1's capacitance Cpd) to generate a voltage at its output that is indicative of the voltage at its input. Nor does Kozlowski teach or suggest that the voltage at amplifier A1's input (or A1's output, which is the left plate of capacitor C_{clamp}) is clamped at a time when amplifier A1's input (or output) receives a sensor current.

The Office Action asserts that Kozlowski's amplifier A2 corresponds to the recited output voltage generation circuitry, and apparently contends that the input node of amplifier A2 corresponds to the recited input node, receives a sensor current, and is clamped at a fixed (or substantially fixed) potential while amplifier A2 generates an output voltage in response to the sensor current.

However, Kozlowski does not teach or suggest (at column 4, lines 15-30) or elsewhere that the input node of amplifier A2, or the output node of amplifier A1, is clamped at a fixed or substantially fixed potential while amplifier A2 generates an output voltage in response to a sensor current. Nor does Kozlowski teach or suggest the input node of amplifier A2 receives a sensor current. Rather, Kozlowski teaches that switches S1 and S2 of Fig. 1 are closed to reset the Fig. 1 circuit (before it circuit enters a sampling mode in which it generates a voltage indicative of the voltage at the input of amplifier A1). Apparently, to enter the sampling mode, switches S1 and S2 are opened. The statement at col. 4, line 15, that switches S1 and S2 are closed to enter the sampling mode is apparently in error since these switches are closed during the reset period prior to the sampling mode. During sampling (with switches S1 and S2 opened) the voltage across capacitor C_{clamp} is clamped, which means that the potential difference between the plates of capacitor C_{clamp} is fixed. However, the potential of each plate of capacitor C_{clamp} necessarily changes during the sampling mode, as the potential at amplifier A1's input changes and the potential at amplifier A2's input changes in response to the changing potential at amplifier A1's input. Neither the potential at amplifier A2's input nor at amplifier A1's output is clamped during sampling. The potential at each plate of capacitor C_{clamp} of Fig. 1 necessarily changes during the sampling period (mode), as the potential at the left plate of capacitor C_{clamp} changes from its initial (reset) value at the start of the sampling period to its final value (indicative of the voltage across PD1 which is in turn indicative of an amount of photogenerated charge).

Nor does Kozlowski teach or suggest any other circuit or method (of the type recited in claim 1 or 54) in which a sensor cell asserts a sensor current to an input node of output voltage generation circuitry (or a readout circuit), and the output voltage generation circuitry (or readout circuit) generates an output voltage in response to the sensor current

while clamping the input node at a potential that is at least substantially fixed.

On the contrary, Kozlowski teaches away from the invention of claims 1 and 54. The circuit of Kozlowski's Fig. 2 includes a source follower (transistor Q21) and circuitry coupled to the source follower for reading out photodiode PD3 by generating (during a sampling period) an output voltage indicative of the current through transistor Q21's channel. There is no teaching or suggestion in Kozlowski that the potential at the source or drain of transistor Q21, or either plate of capacitor C_{clamp} of Fig. 2, or any other node of Fig. 2 that arguably corresponds to the recited input node, is clamped during the sampling period. On the contrary, the potential at each plate of capacitor C_{clamp} of Fig. 2 necessarily changes during the sampling period, as the potential at the left plate of capacitor C_{clamp} changes from its initial (reset) value (at the start of the sampling period) to its final value that is indicative of transistor Q21's gate potential (and thus indicative of a voltage across PD3 that is in turn indicative of an amount of photogenerated charge). During the sampling period, transistor Q23 of Fig. 2 is off, so that the voltage across capacitor C_{clamp} is clamped which implies that the potential difference between the plates of capacitor C_{clamp} is fixed and the potential at the gate of transistor Q24 is capacitively coupled to (and thus follows) the potential at the left plate of capacitor C_{clamp}. Kozlowki's Fig. 2 circuit could not function to generate an output signal indicative of transistor Q21's channel current if the potential at either plate of capacitor C_{clamp} were clamped at a fixed or substantially fixed potential during sampling.

As explained above, Kozlowski fails to teach or suggest output voltage generation circuitry (as recited in claim 1) configured to generate an output voltage in response to a sensor current at an input node while clamping the input node at a potential that is at least substantially fixed, or a method (as recited in claim 54) comprising the steps of asserting a sensor current (indicative of a sensed value) from a sensor cell to an input node of a readout circuit; and operating the readout circuit in response to the sensor current to generate an output voltage (indicative of a sensed value) while clamping the input node at a potential that is at least substantially fixed, and Kozlowski instead teaches away from the invention of claims 1 and 54. Accordingly, Applicants respectfully contend that claims 1 and 54 and all claims that depend directly or indirectly therefrom are patentable over Kozlowski.

Claims 1-5 and 54 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,929,434 (Kozlowski '434). In response, Applicants respectfully contend that claims 1 and 54 (and all claims that depend directly or indirectly from claim 1 or 54) are patentable over Kozlowski '434 for the following reasons.

Kozlowski '434 discloses a circuit including photodiode 10 and a current mirror (comprising transistors 12 and 14) for generating an output current (the current through the channel of transistor 14) in response to a sensor current (the current through the channel of transistor 12). Kozlowski '434 teaches that transistor 12's gate-to-source voltage "self-adjusts" in response to the value of the sensor current. Transistor 14's gate-to-source voltage (and gate potential) changes in response to changes in transistor 12's gate-to-source voltage (and gate potential). Kozlowski '434 does not teach or suggest, and the Examiner does not contend that it does, clamping the gate potential of transistor 12 (and thus the gate potential of transistor 14) during generation of the output current, or operating a readout circuit in response to a sensor current (indicative of a sensed value) to generate an output voltage (indicative of the sensed value) while clamping an input node of the readout circuit at a potential that is at least substantially fixed as recited in claim 54. Kozlowski '434's circuit would not function as intended if the gate potential of transistor 12 (and transistor 14) were clamped during generation of the output current. Since the source of transistor 14 is held a fixed potential, clamping the gate potential of transistor 12 (and thus that of transistor 14) would fix the output current through transistor 14's channel at single value, so that this output current would not be indicative of a sensor current (i.e., a sensor current indicative of photogenerated charge on photodiode 10). Thus, Kozlowski '434 teaches away from the invention of claims 1 and 54.

Applicants contend that there is no basis determinable from Kozlowski '434 or any other reference of record in support of the assertion in the Office Action that it "would have been obvious for one of ordinary skill in the art to modify Kozlowski '434 by adding [sic] clamping the input node" at a fixed (or substantially fixed) potential. Kozlowski '434's teaching of a high gain amplifier 16 between the source and gate of transistor 12 in is inconsistent with a teaching or suggestion to clamp transistor 12's gate potential, and is instead a teaching away from a clamping transistor 12's gate at a fixed or substantially fixed potential. The function of amplifier 16 is to cause transistor 12's gate potential to

vary (in response to changing channel current through transistor 12) at a rate appropriate to the magnitude of the incident photon flux at photodiode 10. As explained in Kozlowski '434 (e.g., at col. 2, lines 34-41 and col. 3, lines 35-58), amplifier 16 decreases or increases the RC time constant with which transistor 12's gate potential varies in response to changes in transistor 12's channel current, but amplifier 16 does not prevent transistor 12's gate potential from changing in response to changing channel current through transistor 12. Transistor 12's gate potential must change in response to changing channel current through transistor 12 for Kozlowski '434's circuit to function as intended. If transistor 12's gate potential were clamped at a fixed value (independent of the channel current through transistor 12), the circuit's output current (the current through transistor 14's channel) would not be indicative of a sensor current (i.e., a sensor current indicative of photogenerated charge on photodiode 10).

All claims that depend directly or indirectly from claim 1 are patentable over Kozlowski '434 for the same reasons (set forth above) that claim 1 is patentable over Kozlowski '434, and all claims that depend directly or indirectly from claim 54 are patentable over Kozlowski '434 for the same reasons (set forth above) that claim 54 is patentable over Kozlowski '434 .

An independent reason that claims 2 and 3 are patentable over Kozlowski '434 is that Kozlowski '434 fails to teach or suggest output voltage generation circuitry including a differential pair as recited in claim 2. Contrary to the apparent suggestion in the Office Action, the circuit of Kozlowski '434's Fig. 6 is not an output voltage generation circuit. Instead, it is an implementation of amplifier 16 of Kozlowski '434's Fig. 1.

Claims 5 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski '434 in view of U.S. 4,816,768 (Champlin). In response, Applicants contend that claims 5 and 6 are patentable over the cited references for the following reasons.

Claims 5 and 6 are patentable over Kozlowski '434 for the same reasons (set forth above) that claim 1 is patentable over Kozlowski '434. Champlin, like Kozlowski '434, fails to teach or suggest clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node)

as recited in claim 1. Thus, claim 1, and claims 5 and 6, are patentable over Champlin considered alone.

There is no teaching or suggestion determinable from Champlin to modify Kozlowski '434's teaching by clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node) as recited in claim 1. Thus, claim 1, and claims 5 and 6, are patentable over the combined teaching of Kozlowski '434 and Champlin, considered individually or in combination.

Claims 7 and 55-58 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kozlowski '434 in view of U.S. 6,791,613 (Shinohara). In response, Applicants contend that these claims are patentable over the cited references for the following reasons.

Claim 7 is patentable over Kozlowski '434 for the same reasons (set forth above) that claim 1 is patentable over Kozlowski '434. Shinohara, like Kozlowski '434, fails to teach or suggest clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node) as recited in claim 1. Thus, claim 1 (and thus claim 7) is patentable over Shinohara considered alone.

There is no teaching or suggestion determinable from Shinohara to modify Kozlowski '434's teaching by clamping an input node of output voltage generation circuitry (configured to generate an output voltage in response to a sensor current at the input node) as recited in claim 1. Thus, claim 1, and claim 7, are patentable over the combined teaching of Kozlowski '434 and Shinohara, considered individually or in combination.

Each of claims 55-58 is patentable over Kozlowski '434 for the same reasons (set forth above) that claim 54 is patentable over Kozlowski '434. Shinohara, like Kozlowski '434, fails to teach or suggest operating a readout circuit in response to a sensor current (indicative of a sensed value) to generate an output voltage (indicative of the sensed value) while clamping an input node of the readout circuit at a potential that is at least substantially

fixed as recited in claim 54. Thus, claim 54 (and thus claims 55-58) are patentable over Shinohara considered alone.

There is no teaching or suggestion determinable from Shinohara to modify Kozlowski '434's teaching by operating a readout circuit in response to a sensor current (indicative of a sensed value) to generate an output voltage (indicative of the sensed value) while clamping an input node of the readout circuit at a potential that is at least substantially fixed as recited in claim 54. Thus, claim 54, and claims 55-58, are patentable over the combined teaching of Kozlowski '434 and Shinohara, considered individually or in combination.

Reconsideration and allowance of the rejected claims is respectfully requested.

Respectfully submitted,
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